COMPLETE LISTING OF THE CLAIMS

The following lists all of the claims that are or were in the above-identified patent application. The status identifiers respectively provided in parentheses following the claim numbers indicate the current statuses of the claims.

1. (Previously Presented) A probing system for testing a device comprising:

a probe comprising a semiconductor die and probe tips rigidly attached to the semiconductor die, wherein the probe tips comprise bumps that are arranged in a pattern that matches a pattern of terminals on the device and that directly contact the terminals during testing of the device, the probe tips being affixed to the semiconductor die so that the pattern of the probe tips expands/contracts with thermal expansion/contraction of the semiconductor die;

a substrate on which the semiconductor die is mounted;

a probe card including a receptacle sized to hold the substrate, wherein the substrate is detachably mounted in the receptacle; and

a tester electrically connected to the probe tips.

- 2. (Original) The system of claim 1, wherein the device comprises a semiconductor material that is substantially the same as material in the semiconductor die.
 - 3. (Canceled)
 - 4. (Canceled)
- 5. (Previously Presented) The system of claim 1, wherein the substrate is substantially identical to a substrate used in a flip-chip package for the device.
 - 6. (Canceled)
- 7. (Original) The system of claim 1, wherein the semiconductor die comprises: terminals on a bottom surface of the semiconductor die; and conductive vias that pass through the semiconductor die and provide electrical connections between the probe tips on a top surface of the die and the terminals on the bottom

PATENT LAW OFFICE OF DAVID MILLERS 1221 SUN RIDGE ROAD PLACERVILLE, CA 95667 PH: (530) 621-4545 FX: (530) 621-4543 surface.

8. (Previously Presented) The system of claim 7, wherein the terminals of the semiconductor die directly contact the substrate.

9. (Previously Presented) The system of claim 8, wherein terminals on the substrate directly contact the probe card.

10. (Original) The system of claim 1, further comprising a positioning system adapted to position the probe relative to the device so that the probe tips contact the terminals on the device.

Claims 11-28 (Canceled)

29. (Previously Presented) The system of claim 1, further comprising contact pads that are directly on the semiconductor die, wherein the bumps respectively reside on the contact pads.

- 30. (Previously Presented) The system of claim 29, wherein the contact pads have a pattern identical to corresponding contact pads on the device tested.
- 31. (Previously Presented) The system of claim 1, wherein surfaces of the bumps that contact the device are planar and in the same plane.
- 32. (Previously Presented) The system of claim 1, wherein the semiconductor die is substantially identical to the device.
- 33. (Previously Presented) The system of claim 1, wherein the bumps are of a type suitable for use in a flip-chip package.
- 34. (Previously Presented) The system of claim 5, wherein the semiconductor die comprises:

terminals on a bottom surface of the semiconductor die arranged in a pattern that -3-

PATENT LAW OFFICE OF 1221 SUN RIDGE ROAD ACERVILLE, CA 95667 PH: (530) 621-4545

matches the pattern of the terminals on the device; and

conductive vias that pass through the semiconductor die and provide electrical connections between the probe tips on a top surface of the semiconductor die and the terminals on the bottom surface.

35. (Previously Presented) The system of claim 1, wherein solder attaches the semiconductor die to the substrate.

PATENT LAW OFFICE OF DAVID MILLERS 1221 SUN RIDGE ROAD PLACERVILLE, CA 95667

PH: (530) 621-4545 FX: (530) 621-4543